G. PULLA REDDY ENGINEERING COLLEGE (Autonomous): KURNOOL

Accredited by NBA of AICTE and NAAC of UGC with A Grade,

Affiliated to JNTUA, Anantapuramu

Scheme – 2023

Scheme and Syllabus for

B. Tech. HONORS
in
Electronics and Communication Engineering

Offered by

Department of Electronics and Communication Engineering

G. PULLA REDDY ENGINEERING COLLEGE (AUTONOMOUS): KURNOOL

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

HONORS in ECE (for ECE students only)

(Effective for the students admitted from the academic year 2023-2024 onwards)

S. No	Course Code	Course Title	Credits	Scheme of Instruction periods/week		Scheme of Examination Maximum Marks		
				L	T/P	End Exam Assessment	Internal Assessment	Total (100M)
1	HEC01	Analog IC Design	3	3	0	70	30	100
2	HEC02	Digital IC Design	3	3	0	70	30	100
3	HEC03	Analog and Digital IC Design Lab	1.5	0	3	70	30	100
4	HEC04	Advanced Low Power VLSI	3	3	0	70	30	100
5	HEC05	Testing and Verification	3	3	0	70	30	100
6	HEC06	Physical Design Automation Lab	1.5	0	3	70	30	100
7	HEC07	FPGA & ASIC Architectures	3	3	0	70	30	100
	Total		**18**					

ANALOG IC DESIGN (AID)

V Semester: ECE								Scheme:2023
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEC01	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	30	70	100
Sessional Exam Duration: 2 Hrs						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Understand the MOSFET characteristics, biasing techniques and current mirrors for analog circuit design.

CO2: Design single-stage amplifiers and their performance with feedback and cascode configurations.

CO3: Analyze the design and performance of differential amplifiers in analog circuits.

CO4: Learn the characteristics and compensation techniques of operational amplifiers.

CO5: Understand the design principles of bandgap reference circuits.

UNIT – I

`Review of MOSFET device characteristics: Second order effects, MOS small signal Model, Capacitances, body bias effect, Current biasing, voltage biasing, Technology biasing, Relative comparison and limitations. Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Mismatch in accuracies, Design solutions to minimize mismatch in accuracies.

UNIT – II

Single stage amplifier: Analytical justification of operating region suitable for amplification/switching ,Design of CS amplifier with different loads, Limitations of diode connected load, Improving output impedance of CS amplifier through feedback ,small signal analyses of common gate and common drain topologies and their frequency response with parasitic affects, significance of cascode, design of cascade amplifier and with ideal current source load and practical cascode load, Limitations of cascode, folded cascode amplifier and design with parasitics.

UNIT – III

Differential amplifier: Significance of differential signaling, Limitations of quasi differential amplifier, Design of differential amplifier with current source load and diode connected load and small signal analyses, errors due to mismatch, replication principle, qualitative analysis, common mode response, gilbert cell, Common centroid layout.

UNIT – IV

Operational amplifier: Characterization, two stage OP-amp, small signal analysis, Miller compensation, effect of RHP zero on stability, Lead compensation, constant gm biasing, design of biasing circuit independent of process and temperature variations.

UNIT – V

Band Gap Reference: General considerations, Supply independent biasing, temperature independent references, negative-TC voltage, positive TC voltage, Bandgap reference, PTAT generation, curvature correction, Design of BGR under low voltage conditions.

Textbooks:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education,2017,2nd Edition
2. Paul J. Hurst, Paul R. Gray, Robert G Meyer and Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, 6thEdition..

3. Mohammed Ismail and TerriFiez, Analog VLSI: Signal and Information Processing, McGraw Hill, 1994.

References:

1. Randall L. Geiger, Phillip E. Allenand Noel R. Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 1989.
2. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2ndEdition.
3. Paul G. A. Jesper and Boris Murmann, Systematic Design of Analog CMOS Circuits, Cambridge University Press, 2017.

Question Paper Pattern:

Sessional Exam:

The question paper for Sessional Examination shall be for 40 marks. The question paper shall consist of Four questions and all questions are compulsory. Question No.1 contains Five short answer questions (2 marks each) for a total of Ten marks. Remaining Three questions shall be EIHER/OR Type descriptive questions for Ten marks each. Each of these descriptive questions may contain sub-questions.

End Examination:

The question paper for End Examination shall be for 70 marks. The Question paper shall contain Six Questions and all questions are compulsory. Question No.1 shall contain Ten short answer questions (2 marks each) for a total of Twenty marks, with Two short answer questions from each unit. Remaining Five Questions (Each question covering one unit of syllabus) carrying 10 marks each shall be EITHER/OR Type descriptive questions and may contain sub-questions.

DIGITAL IC DESIGN (DID)

V Semester: ECE						Scheme:2023		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEC02	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	30	70	100
Sessional Exam Duration: 2 Hrs						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Understand MOSFET and CMOS inverter operation along with constraints.

CO2: Explore CMOS design techniques for combinational and sequential logic circuits.

CO3: Evaluate different design approaches to mitigate timing issues in digital circuits.

CO4: Design arithmetic building blocks for digital systems.

CO5: Design a basic memory subsystem.

UNIT – I

MOS Inverters: Structure and Operation of MOS Transistor (MOSFET), MOSFET Current Voltage Characteristics, MOSFET Scaling and Small-Geometry Effect, MOSFET Capacitances, CMOS Inverter-Static and switching characteristics, Delay-Time Definitions, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitic, Power Consumption in CMOS Gates.

UNIT – II

Designing Combinational & Sequential Logic Gates in CMOS: Static CMOS design- ratioed logic, pass transistor logic, transmission gate logic, Dynamic CMOS Design, Static Latches and Registers, Dynamic Latches and Registers, Alternative Register Styles, Non bi-stable Sequential Circuits, Logic Style for Pipelined Structures.

UNIT – III

Timing Issues in Digital Circuits: Introduction, Synchronous Timing basics, Clock Skew and Jitter, Clock distribution techniques, Clock Generation and Synchronization.

UNIT – IV

Designing Arithmetic Building Blocks: Introduction, The Adder: Circuit and Logic Design, Multipliers: Shifters, Power Considerations in Data path Structures.

UNIT – V

Designing Memory: Introduction, Semiconductor Memories - An Introduction, The Memory Core: RAM, ROM, and Memory Peripheral Circuitry.

Textbooks:

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson, 2003, 2ndEdition
2. John P. Uyemura, CMOS Logic Circuit Design, Springer,2001.
3. John P. Uyemura, Introduction to VLSI Circuits and Systems, Wiley,2002.

References:

1. Sung-MoKangandYusufLeblebici,CMOSDigitalIntegratedCircuits,McGraw-Hill, 2003,3rdEdition
2. Charles Hawkins, Jaume Seguraand Payman Zarkesh Ha, CMOS Integrated Digital Electronics: A First Course, IET, 2012.

Question Paper Pattern:

Sessional Exam:

The question paper for Sessional Examination shall be for 40 marks. The question paper shall consist of Four questions and all questions are compulsory. Question No.1 contains Five short answer questions (2 marks each) for a total of Ten marks. Remaining Three questions shall be EIHER/OR Type descriptive questions for Ten marks each. Each of these descriptive questions may contain sub-questions.

End Examination:

The question paper for End Examination shall be for 70 marks. The Question paper shall contain Six Questions and all questions are compulsory. Question No.1 shall contain Ten short answer questions (2 marks each) for a total of Twenty marks, with Two short answer questions from each unit. Remaining Five Questions (Each question covering one unit of syllabus) carrying 10 marks each shall be EITHER/OR Type descriptive questions and may contain sub-questions.

ANALOG AND DIGITAL IC DESIGN LAB (ADID(P))

V Semester: ECE								Scheme:2023
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEC03	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		0	0	3	1.5	30	70	100
						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Evaluate single-stage and multi-stage amplifiers with various loads and feedback techniques.

CO2: Apply the principles of current sources, sink, and mirrors for effective circuit biasing.

CO3: Implement CMOS differential and two-stage operational amplifiers through post-layout simulations.

CO4: Analyze CMOS inverters and logic gates with different design constraints and logic styles for the performance-optimized design of parallel adders, shift registers, and multipliers.

CO5: Verify digital systems through functional simulation, static timing analysis, and post-synthesis verification.

List of Experiments

PART A (Analog IC Design Lab)

1. Lambda calculation for PMOS & NMOS, Transconductance plots,
2. Single transistor amplifier with different loads
3. CS amplifier with source degeneration
4. Cascode amplifier
5. Basic current sink, Cascode current sink
6. Basic current source, Cascode current source
7. Basic current mirror, Wilson current mirror
8. Cascode current mirror
9. Feedback topologies
10. CMOS differential amplifier with current mirror load
11. Two stage Operational amplifier

Note: Any five experiments from each group (All circuit still post layout)

PART B (Digital IC Design Lab)

1. Design and Simulation of CMOS Inverter to study the transfer Characteristics by varying the design constraints using EDA Tools
2. Design and Simulation of logic gates using various logic styles and compare the performance

Design the following building blocks employing various architectures and develop HDL models:

3. 32-bit Parallel adder using 8-bit adder module

4. 32-bit Shift register using 8-bit Shift register module

5. Combinational and sequential multipliers: 8 x 8 multiplier

6. Combinational and sequential multipliers: 16 X 16 multipliers

7. Perform the functional simulation, Static Timing Analysis and post synthesis timing verification RTL to GDS-II: Design any System as a case Study

Textbooks:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuit, McGraw Hill Education, 2017, 2nd Edition Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Pearson, 2003, 2ndEdition
2. Paul J. Hurst, Paul R. Gray, Robert G Meyerand Stephen H. Lewis, Analysis and Design of Analog Integrated Circuits, Wiley, 2024, 6th Edition
3. Samir Palnitkar, Verilog HDL, Pearson Education, 2003, 2nd Edition.
4. ErikBrunv and, Digital VLSI Chip Design with Cadence and Synopsys CAD Tools, Pearson, 2011.

References:

1. Randall L. Geiger, Phillip E. Allen and Noel R. Strader, VLSI Design Techniques for Analog and Digital Circuits, Tata McGraw-Hill Education, 1989.
2. David Johns, Tony Chan Carusone and Kenneth Martin, Analog Integrated Circuit Design, Wiley, 2011, 2ndEdition.
3. Joseph Cavanagh, Verilog HDL Design Examples, CRC Press,2018.
4. Blaine Readler, Verilog by Example: A Concise Introduction for FPGA Design, Full ARC Press,2011

Advanced Low Power VLSI (ALPV)

VI Semester: ECE						Scheme:2023		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEC04	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	30	70	100
Sessional Exam Duration: 2 Hrs						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Explore low-power CMOS VLSI design techniques for minimizing power dissipation.

CO2: Understand CMOS adder architectures and low-power design techniques.

CO3: Analyze various multiplier architectures and low-power design techniques for memories.

CO4: Examine architectural techniques for minimizing power dissipation in digital systems.

CO5: Apply low-power design techniques for optimizing power consumption in digital circuits.

UNIT – I

Low Power CMOS VLSI design: Introduction: Sources of Power Dissipation, Static Power Dissipation, Active Power Dissipation.

Circuit Techniques for Low Power Design: Design for Low Power, Multiple Vth techniques, Dynamic Vth techniques.

UNIT – II

Adders: Standard Adder Cells, Review of CMOS Adders Architectures and performance Comparison, Low Voltage Low Power Design Techniques, Current Mode Adders.

UNIT – III

Multipliers and Memories: Review of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison. Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques.

UNIT – IV

Architectural Techniques for Low Power: Parameters effecting power dissipation, Variable frequency, Dynamic voltage Scaling, Dynamic Voltage and Frequency Scaling, Reduced VDD, Architectural clock gating, Power gating, Multi-voltage, Optimizing memory power.

UNIT – V

Low Power Implementation Techniques: Library Selection, Clock Gating, Timing Impact due to Clock gating, Gate-level power optimization techniques, Power Optimization for Sleep Mode.

Textbooks:

1. Kiat Seng Yeo and Kaushik Roy, Low-Voltage, Low-Power VLSI Subsystems, Tata McGraw Hill, 2009
2. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002.

References:

1. Abdellatif Bellaouar, Mohamed Elmasry, Low Power Digital VLSI Design: Circuits and Systems, Springer, 2012.
2. Jan Rabaey, Low Power Design Essentials,Springer,2009.

Question Paper Pattern:

Sessional Exam:

The question paper for Sessional Examination shall be for 40 marks. The question paper shall consist of Four questions and all questions are compulsory. Question No.1 contains Five short answer questions (2 marks each) for a total of Ten marks. Remaining Three questions shall be EIHER/OR Type descriptive questions for Ten marks each. Each of these descriptive questions may contain sub-questions.

End Examination:

The question paper for End Examination shall be for 70 marks. The Question paper shall contain Six Questions and all questions are compulsory. Question No.1 shall contain Ten short answer questions (2 marks each) for a total of Twenty marks, with Two short answer questions from each unit. Remaining Five Questions (Each question covering one unit of syllabus) carrying 10 marks each shall be EITHER/OR Type descriptive questions and may contain sub-questions.

TESTING AND VERIFICATION (T&V)

VI Semester: ECE						Scheme:2023		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEC05	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		3	0	0	3	30	70	100
Sessional Exam Duration: 2 Hrs						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1- Analyze testing methods for improving VLSI chip quality and yield.

CO2- Apply fault simulation algorithms for testing and diagnosing faults in digital systems.

CO3- Implement test pattern generation techniques for fault detection in combinational and sequential circuits .

CO4- Develop and deploy optimized fault detection strategies for digital systems, leveraging ATPG algorithms and integrating Design-for-testability (DFT) practices.

CO5- Utilize DFT methodologies to enhance testability, generate test patterns, and implement BIST for efficient fault detection in digital systems.

UNIT – I

Role of testing in VLSI Design flow, Testing at different levels of abstraction, Fault, error, defect, diagnosis, yield, Types of testing, Rule of Ten, Defects in VLSI chip. Modelling basic concepts, Functional modelling at logic level and register level, structure models, logic simulation, delay models. Various types of faults, Fault equivalence and Fault dominance in combinational sequential circuits.

UNIT – II

Fault simulation applications, General fault simulation algorithms- Serial, and parallel, Deductive fault simulation algorithms.

UNIT – III

Combinational circuit test generation, Structural Vs Functional test, ATPG, Path sensitization methods. Difference between combinational and sequential circuit testing, five and eight valued algebra, and Scan chain-based testing method.

UNIT – IV

D-algorithm procedure, Problems, PODEM Algorithm. Problems on PODEM Algorithm. FAN Algorithm. Problems on FAN algorithm, Comparison of D, FAN and PODEM Algorithms. Design for Testability, Ad-hoc design, Generic scan-based design.

UNIT – V

Classical scan-based design, System level DFT approaches Test pattern generation for BIST, Circular BIST. BIST Architectures. Testable memory Design-Test Algorithms-Test generation for Embedded RAMs.

Textbooks:

1. M. Abramovici, M. Breuer, and A. Friedman, ―Digital Systems Testing and Testable Design, IEEE Press, 1990.
2. M. Bushnell and V. Agrawal, ―Essentials of Electronic Testing for Digital, Memory & Mixed-Signal VLSI Circuits‖, Kluwer Academic Publishers, 2000.

References:

1. Stroud,—A Designer‘s Guide to Built-in Self-Test’, Kluwer Academic Publishers, 2002
2. V. Agrawaland S.C. Seth, Test Generation for VLSI Chips, Computer Society Press.1989

Question Paper Pattern:

Sessional Exam:

The question paper for Sessional Examination shall be for 40 marks. The question paper shall consist of Four questions and all questions are compulsory. Question No.1 contains Five short answer questions (2 marks each) for a total of Ten marks. Remaining Three questions shall be EIHER/OR Type descriptive questions for Ten marks each. Each of these descriptive questions may contain sub-questions.

End Examination:

The question paper for End Examination shall be for 70 marks. The Question paper shall contain Six Questions and all questions are compulsory. Question No.1 shall contain Ten short answer questions (2 marks each) for a total of Twenty marks, with Two short answer questions from each unit. Remaining Five Questions (Each question covering one unit of syllabus) carrying 10 marks each shall be EITHER/OR Type descriptive questions and may contain sub-questions.

PHYSICAL DESIGN AUTOMATION LAB (PDA(P))

VI Semester: ECE						Scheme:2023		
Course Code	Category	Hours/Week			Credits	Maximum Marks		
HEC06	PC	L/D	T	P	C	Continuous Internal Assessment	End Exam	Total
		0	0	3	1.5	30	70	100
						End Exam Duration:3 Hrs		

Course Outcomes:

After the completion of the course students will be able to

CO1: Apply graph-based algorithms to solve problems like spanning trees, shortest paths, and Steiner trees in VLSI design.

CO2; Analyze line sweep and extended line sweep methods for geometric problem-solving.

CO3; Apply partitioning techniques to optimize circuit design using algorithms like Kernighan-Lin, simulated annealing, and metric allocation.

CO4: Utilize floor planning algorithms to optimize area, performance, and layout efficiency in VLSI design.

CO5: Implement two-terminal and multi-terminal routing algorithms for optimal interconnection in circuits and networks.

List of Experiments

Note: Any ten experiments are to be conducted (Minimum one from each group)

I. Graph algorithms

1. Graph search algorithms
   - Depth first search
   - Breadth first search
2. Spanning tree algorithm
   - Kruskal‘s algorithm
3. Shortest path algorithm
   - Dijkstra algorithm
   - Floyd-Warshall algorithm
4. Steiner tree algorithm

II. Computational geometry algorithm

1. Line sweep method
2. Extended line sweep method

III. Partitioning algorithms

1. Group migration algorithms
   - Kernighan –Lin algorithm
   - Extensions of Kernighan-Lin algorithm

- Fiduccias –Mattheyses algorithm
- Goldberg and Burstein algorithm

2. Simulated annealing and evolution algorithms
   - Simulated annealing algorithm
   - Simulated evolution algorithm
3. Metric allocation method

IV. Floor planning algorithms

1. Constraint based methods
2. Integer programming based methods
3. Rectangular dualization based methods
4. Hierarchical tree based methods
5. Simulated evolution algorithms
6. Time driven Floor planning algorithms

V. Routing algorithms

1. Two terminal algorithms
   - Maze routing algorithms
     - Lee ‘s algorithm
     - Souk up ‘s algorithm
     - Hadlock algorithm
   - Line-Probe algorithm
   - Shortest path based algorithm

2.Multi terminal algorithm

- Stenier tree based algorithm
  - SMST algorithm
  - Z-RST algorithm

FPGA & ASIC ARCHITECTURES

VII Semester: ECE						Scheme:2023		
Course Code	Course Category	Hours/Week			Credits	Maximum Marks		
HEC07	PC	L	T	P	C	Continuous Internal Assessment	End Exam	TOTAL
		3	0	0	3	30	70	100
Sessional Exam Duration:2Hrs						End Exam Duration: 3Hrs		

Course Outcomes:

At the end of the course the student will be able to

CO1 Implementation of ROMs, PALs, PLAs, CPLDs

CO2: Apply &Get exposure to industry standard FPGAs

CO3: Analyze the concepts of FPGAs design Flow and its I/O Blocks

CO4: Understand the concepts of ASICs and its design Flow.

CO5: Analyze system partitioning, floor-planning Placement & Routing and associated algorithms

UNIT-I

Basics of FPGA:
Programmable logic, Programmable read only memory (PROM), programmable logic array (PLA), Programmable array logic (PAL). Sequential programmable logic devices (SPLDS), Programmable gate arrays (PGAS), CPLD

UNIT-II

Programmable logic FPGA general structure, Anti fuse - Static RAM: EPROM and EEPROM technology, FPGA Logic block – ZYNQ 7000

UNIT-III

FPGA Design flow , DC & AC inputs and outputs, Clock and Power inputs, Xilinx I/O blocks.

UNIT-IV

ASIC construction: Physical Design flow , Goals and objectives of all the ASIC physical design steps, System partitioning, Partitioning method—Constructive partitioning, Iterative partitioning, K-L algorithm.

UNIT-V

Floor planning, its tools, Placement : Methods and types-- constructive: min-cut placement method, Eigenvalue placement algorithm, Iterative Placement Improvement..

Text Books:

1. Michael John Sebastian Smith, Application specific Integrated Circuits, 3 rd Edition, Pearson Education, Asia, 2001.
2. Pak and Chan, Samiha Mourad, Digital Design using Field Programmable Gate Arrays, 1st Edition Pearson Education, 2009.

Reference Books:

1. S. Trimberger, Edr, Field Programmable Gate Array Technology, 1st Edition Kluwer Academic Publications,1994.
2. John V. Oldfield, Richard C Dore, Field Programmable Gate Arrays, 1 st Edition,Wiley Publications,1999.

3. S. Brown, R Francis, J Rose, Z Vransic, Field Programmable Gate Arrays, 1 st edition, Kluwer Publications, 1992

Web References:

1. https://nptel.ac.in/courses/117108040/
2. https://www.coursera.org/learn/intro-fpga-design-embedded-systems/
3. http://www.cpld.com/
4. www.asic.co.in/

Question Paper Pattern:

Sessional Exam:

The question paper for Sessional Examination shall be for 40 marks. The question paper shall consist of Four questions and all questions are compulsory. Question No.1 contains Five short answer questions (2 marks each) for a total of Ten marks. Remaining Three questions shall be EIHER/OR Type descriptive questions for Ten marks each. Each of these descriptive questions may contain sub-questions.

End Examination:

The question paper for End Examination shall be for 70 marks. The Question paper shall contain Six Questions and all questions are compulsory. Question No.1 shall contain Ten short answer questions (2 marks each) for a total of Twenty marks, with Two short answer questions from each unit. Remaining Five Questions (Each question covering one unit of syllabus) carrying 10 marks each shall be EITHER/OR Type descriptive questions and may contain sub-questions